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10/557,746	11/21/2005	Satoshi Shibata	071971-0432	2300

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EXAMINER	
CRAWFORD, LATANYA N	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any; is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/557,746	SHIBATA, SATOSHI	
	Examiner	Art Unit	
	LaTanya Crawford	2809	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/21/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1,2,5,7,9, &11** are rejected under 35 U.S.C. 102***(b)*** as being anticipated by **Yu (US Patent 6,521,502 B1).**

Regarding Claim 1, Yu et al. discloses a method for manufacturing a semiconductor device, comprising the steps of: forming an amorphous layer **25** in a region from a surface of a semiconductor region **12** to a first depth **(FIG. 2; column 5, lines 8-9 & lines 31-36)**; by heat treating the amorphous layer at a prescribed temperature, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth **(Fig. 3; column 6, lines 46-48; lines 58-59)**; and forming a pn junction at a third depth that is shallower than the second depth by introducing ions into the heat-treated amorphous layer **(fig 1; column 5, lines 54-58)**.

Regarding claim 2, Yu et al. discloses wherein the prescribed temperature is in a range of 475°C to 600°C **(column 6, lines 58-59)**.

Regarding claim 5, a method for manufacturing a semiconductor device, comprising the steps of: forming an amorphous layer **25** in a region from a surface of a semiconductor region **12** of a first conductivity type to a first depth **(FIG. 2; column 5, lines 8-9 & lines 31-36)**; by heat treating the amorphous layer at a prescribed temperature, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth **(Fig. 3; column 6, lines 46-48; lines 58-59)**; forming a first impurity layer **20 and 22 (regions 16 and 18)** of a second conductivity type **(column 4, lines 43-48 & lines 64-65)** which has a pn junction **20 and 22** at a third depth that is shallower than the second depth by introducing ions into the heat-treated amorphous layer **(fig. 1; column 5, lines 54-58)**; and activating the first impurity layer **(column 5, lines 1-3)**.

Regarding claim 7, wherein the prescribed temperature is in a range of 475°C to 600°C **(column 6, lines 58-59)**, and the activation of the first impurity layer is conducted in a temperature range of 500°C to 700°C **(column 6, lines 64-67)**.

Regarding claim 9, a method for manufacturing a semiconductor device, comprising the steps of: forming a gate electrode **30** on a semiconductor region **12** of a first conductivity type **(column 4; line 13)**; forming an amorphous layer **25** in a region from a surface of the semiconductor region **12** of the first conductivity type to a first depth **(FIG. 2; column 5, lines 8-9 & lines 31-36)**; by heat treating the amorphous

layer at a prescribed temperature, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth **(Fig. 3; column 6, lines 46-48; lines 58-59)**; forming a first impurity layer **20 and 22 (40 and 42)** of a second conductivity type **(column 4, lines 43-48 & lines 64-65)** which has a pn junction at a third depth that is shallower than the second depth by introducing ions into the heat-treated amorphous layer **(column 4, lines 43-48)**; forming a second impurity layer **50 and 52** of a first conductivity type which has a pn junction **50 and 52** at a level that is shallower than the first depth and deeper than the third depth by introducing ions into the heat-treated amorphous layer **(Fig 4; column 6,lines 8-14)**; and activating the first impurity layer and the second impurity layer **(column 7, lines1-6)**.

Regarding claim 11, wherein the prescribed temperature is in a range of 475°C to 600°C **(column 6, lines 58-59)**, and the activation of the first impurity layer and the second impurity layer is conducted in a temperature range of 500°C to 700°C **(column 6, lines 64-67)**.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 3,6, & 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yu (US Patent 6,521,502 B1)** in view of **Yu (6,472,282 B1)**.

Regarding claim 3, Yu et al. ('502) invention discloses all of the claimed limitations from above but fails to teach wherein the third depth is in a range of 5 nm to 15 nm.

However, Yu et al. ('282) teaches wherein the third depth **20 and 22** is in a range of 5 nm to 15 nm **(column 6; lines 23-24)**.

5. Given the teachings of Yu et al. ('282), it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the integrated circuit device of Yu et al. ('502) with the source/drain extension dopant implant is projected to a depth of 10-15 nm taught by Yu et al. ('282). Doing so would provide control of short channel effects.

Regarding claim 6, Yu et al. ('502) invention discloses all of the claimed limitations from above but fails to teach wherein the third depth is in a range of 5 nm to 15 nm.

However, Yu et al. ('282) teaches wherein the third depth **20 and 22** is in a range of 5 nm to 15 nm **(column 6; lines 23-24)**.

6. Given the teachings of Yu et al. ('282), it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the integrated circuit device of Yu et al. ('502) with the source/drain extension dopant implant is projected to a depth of 10-15 nm taught by Yu et al. ('282). Doing so would provide control of short channel effects.

Regarding claim 10, Yu et al. ('502) invention discloses all of the claimed limitations from above but fails to teach wherein the third depth is in a range of 5 nm to 15 nm.

However, Yu et al. ('282) teaches wherein the third depth **20 and 22** is in a range of 5 nm to 15 nm **(column 6; lines 23-24).**

7. Given the teachings of Yu et al. ('282), it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the integrated circuit device of Yu et al. ('502) with the source/drain extension dopant implant is projected to a depth of 10-15 nm taught by Yu et al. ('282). Doing so would provide control of short channel effects.

8. **Claims 4, 8, & 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yu (US Patent 6,521,502 B1)** in view of **Yu (6,472,282 B1)** as applied to claim(s) above and further in view of **Wu (US Patent 6,391,751).**

Regarding claim 4, Yu et al. ('502) invention as modified by Yu et al. ('282) discloses all of the claimed limitations from above but fails to teach wherein a pattern of a gate electrode that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region.

However, Wu et al. teaches a pattern of a gate electrode **56** that is formed on the semiconductor region **50** is non-uniformly distributed on the semiconductor region **50 (FIG. 1A an 1B;column 1, lines 51-52).**

9. Given the teachings of Wu et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the integrated circuit device of Yu et

al. ('502) with a non-uniformly distributed gate electrode with side walls taught by Wu et al. Doing so would provide insulation to the gate electrode from the source/drain region.

Regarding claim 8, Yu et al. ('502) invention as modified by Yu et al. ('282) discloses all of the claimed limitations from above but fails to teach wherein a pattern of a gate electrode that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region.

However, Wu et al. teaches a pattern of a gate electrode **56** that is formed on the semiconductor region **50** is non-uniformly distributed on the semiconductor region **50** **(FIG.1A and 1B;column 1, lines 51-52).**

10. Given the teachings of Wu et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the integrated circuit device of Yu et al. ('502) with a non-uniformly distributed gate electrode with side walls taught by Wu et al. Doing so would provide insulation to the gate electrode from the source/drain region.

Regarding claim 12, Yu et al. ('502) invention as modified by Yu et al. ('282) discloses all of the claimed limitations from above but fails to teach wherein a pattern of a gate electrode that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region.

However, Wu et al. teaches a pattern of a gate electrode **56** that is formed on the semiconductor region **50** is non-uniformly distributed on the semiconductor region **50** **(FIG. 1A and 1B; column 1, lines 51-52).**

11. Given the teachings of Wu et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the integrated circuit device of Yu et al. ('502) with a non-uniformly distributed gate electrode with side walls taught by Wu et al. Doing so would provide insulation to the gate electrode from the source/drain region.

12. **Claims 13, 14, & 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yu (US Patent 6,521,502 B1)** in view of **Atsuki (US 2002/0068407 A1)**.

Regarding claim 13, Yu et al. ('502) discloses a method for manufacturing a semiconductor device, comprising the steps of: forming a gate electrode **30** on a semiconductor region **12** of a first conductivity type **(column 4; line 13)**; forming an amorphous layer **25** in a region from a surface of the semiconductor region to a first depth **(fig. 2; column 5, lines 8-9 & lines 31-36)**; restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth **(fig. 3; column 6, lines 46-48)**; forming a first impurity layer of a second conductivity type **(column 4, lines 43-48 & lines 64-65)** which has a pn junction **20 and 22 (40 and 42)** at a third depth that is shallower than the second depth by introducing ions on both sides of the gate electrode in the heat-treated amorphous layer **(fig. 1; column 5, lines 54-58 & 63-67)**; and activating the first impurity layer **(column 5, lines 1-3)**but fails to teach forming sidewalls on a side surface while restoring a crystal structure of the amorphous layer caused by a heat treatment of a prescribed temperature.

However, Atsuki et al. teaches forming sidewalls **8** on a side surface while restoring a crystal structure of the amorphous layer caused by a heat treatment of a prescribed temperature **([0016], lines 8-16)**.

13. Given the teachings of Atsuki et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the integrated circuit device of Yu et al. ('502) with forming sidewalls by CVD at a prescribed temperature to progress crystal growth in an amorphous region taught by Atsuki et al. Doing so would provide a reduction in process steps to manufacture the device.

Regarding claim 14, Yu et al. ('502) discloses the manufacturing method of a semiconductor device according to claim 13, further comprising the step of: after the step of forming the first impurity layer **20 and 22 (40 and 42)**, forming a second impurity layer **50 and 52** of a first conductivity type which has a pn junction **50 and 52** at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer **(fig. 4; column 6, lines 8-14 & 16-18)**, wherein the second impurity layer is simultaneously activated in the step of activating the first impurity layer **(column 7, lines 1-6)**.

Regarding claim 16, Yu et al. discloses the prescribed temperature is in a range of 475°C to 600°C **(column 6, lines 58-59)**, and the activation is conducted in a temperature range of 500°C to 700°C **(column 6, lines 64-67)**.

14. **Claims 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Yu (US Patent 6,521,502 B1)** in view of **Atsuki (US 2002/0068407 A1)** as applied to claim(s) above and further in view of **Yu (6,472,282 B1).**

Regarding claim 15, Yu et al. ('502) invention discloses all of the claimed limitations from above but fails to teach wherein the first impurity layer has a depth of 5 nm to 15 nm.

However, Yu et al. ('282) teaches wherein the first impurity layer **20 and 22** has a depth of 5 nm to 15 nm **(column 6; lines 23-24)**.

15. Given the teachings of Yu et al. ('282), it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the integrated circuit device of Yu et al. ('502) with the source/drain extension dopant implant is projected to a depth of 10-15 nm taught by Yu et al. ('282). Doing so would provide control of short channel effects.

16. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Yu (US Patent 6,521,502 B1) in view of Yu (6,472,282 B1)** as applied to claim(s) above and further in view of **Wu (US Patent 6,391,751)**

Regarding claim 17, Yu et al. ('502) invention as modified by Yu et al. ('282) discloses all of the claimed limitations from above but fails to teach wherein a pattern of a gate electrode that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region.

However, Wu et al. teaches a pattern of a gate electrode **56** that is formed on the semiconductor region **50** is non-uniformly distributed on the semiconductor region **50 (FIG. 1A and 1B; column 1, lines 51-52).**

17. Given the teachings of Wu et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the integrated circuit device of Yu et

al. ('502) with a non-uniformly distributed gat electrode with side walls taught by Wu et al. Doing so would provide insulation to the gate electrode from the source/drain region.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are cited for disclosing related limitations of the applicant's claimed and disclosed invention: **Yu et al., Pramanick et al., Robertson et al., & Yamamoto et al.**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaTanya Crawford whose telephone number is (571) 270-3208. The examiner can normally be reached on Monday-Friday 7:30 AM -5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Terrell McKinnon can be reached on (571) 272-4797. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LaTanya Crawford

June 4, 2007

TERRELL L. MCKINNON
SUPERVISORY PATENT EXAMINER